CMOS VLSI Design Technology and SRAM Design System

Assistant Prof. Yasmeen Saundatti
E&C Department, VTU University
Shaikh College of Engineering and Technology,
Bhootramanhatti Belgaum -591156,
Karnataka, INDIA
yasmeen.s88@gmail.com

ABSTRACT- The microscopic dimensions of current silicon integrated circuits make possible the design of digital circuits which may be very complex and yet extremely economical in space, power requirements and cost, and potentially very fast. The area, power and cost aspects have made silicon the dominant fabrication technology for electronics in very wide range. The combination of complexity and speed is very wide ranging for VLSI system in digital processing. The overwhelming majority of VLSI system in silicon utilizes NMOS, CMOS or BICMOS technology [1]. Fast low power SRAMs have become an important and critical component of many VLSI chips. This is especially true for microprocessor, where the on-chip cache sizes are growing with each generation to bridge the increasing divergence in the speeds of the processor and the main memory [1-2]. Simultaneously, power dissipation has become an important consideration both due to the increased integration and operating speeds, as well as due to the explosive growth of battery operated appliances

1. INTRODUCTION:

Memory arrays often account for the majority of transistors in a CMOS system on chip. Random access memory is accessed with an address and has latency independent of the address. In contrast, serial access memories are accessed sequentially so no address is necessary. Random access memory is commonly classified as Read only Memory and Random access memory, they are also called as volatile and non volatile memory. Volatile memory retains its data as long as power is applied, while non volatile memory will hold data indefinitely. Like sequencing elements, the memory cells used in volatile memories can further be divided into static structures and dynamic structures. Static cells use some form of feedback to maintain their state, while dynamic cells use charge stored on a floating capacitor through an access transistor. Charge will leak away through the access transistor even while the transistor is off, so dynamic cells must be periodically read and rewritten to fresh their state. SRAM's are faster and less troublesome, but require more area per bit than their dynamic counterparts DRAM's.

2. METHODOLOGY

An SRAM Cell is the key component used to store binary information. A typical 6T SRAM cell uses two cross coupled inverters. Access transistors enable access to the cell during read operations and provide cell isolation during the not-accessed state. A 6T SRAM cell is designed to provide non destructive read access, write capability and data storage for as long as power supply is on. The flow chart for the design of low power SRAM read write system is as shown in figure 1. The steps involved in designing 6T SRAM cell are given below

Step 1: Choose the appropriate cell ratio for designing an SRAM Cell. Draw the schematic in microwind using 45nm technology. Check and Save the schematic of SRAM Cell.

Step 2: Once the Schematic entry is ready the schematic of 6T SRAM Cell is simulated using microwind. The simulation is carried out to verify the correct functionality of the 6T SRAM Cell design. Write '1' and write '0' operation of the 6T SRAM Cell design is observed.

Step 3: Check if the simulated waveform is obtained correctly after step 2 if not go back to step 1 and check the circuit design and specifications.

Step 4: Draw the layout of 6T SRAM Cell design. The layout of an SRAM cell defines the area density of the array and is key to manufacturing yield of the SOC containing large SRAM arrays.

Step 5: Layout verification is performed to ensure the layout passes DRC (Design Rule Check) for getting no errors. The layout should also match with the schematic (LVS). Resistance and Capacitance of the SRAM Layout is also extracted using cadence assura RCX.

Step 6: Check if the layout passes DRC, LVS, and RCX correctly if not go back to step 4 until the required flow is achieved.

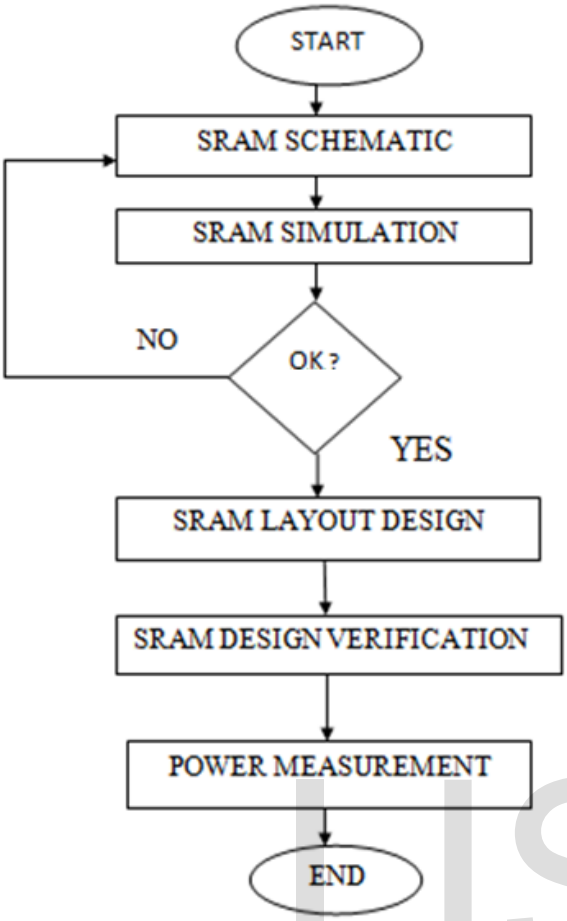

Figure 1: Flow chart for the design of low power SRAM read write system

3. Basic 6T SRAM cell:

It consists of pair of cross coupled inverters that use positive feedback to store value. Transistors M5 and M6 are 2 pass transistors that allow access to the storage nodes for reading and writing. To write a value into a SRAM cell the new value and its complement is driven on the bit lines and then the word line is raised. The new will overwrite the old value, since the bit lines are actively driven by write circuitry. To read a value from an SRAM the bit lines are pre charged high and the word line is raised turning on the pass transistors. Because one of the internal storage nodes is low, one of the bit lines starts discharging. A sense amplifier which is connected to the bit line senses which of the bit line is discharging and reads the stored value. The 6T SRAM cell is designed such that the pull up p-transistors are weakest, access transistors are of medium strength and pull-down nmos transistors are strongest to satisfy write and read constraints. The 6T SRAM cell is as shown in figure 2.

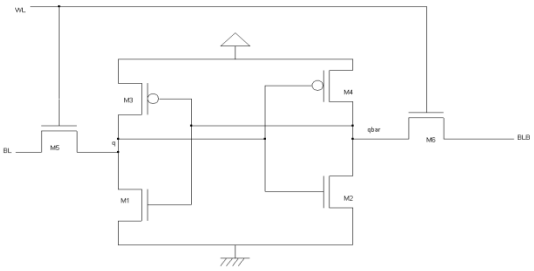

Figure2. 6T SRAM Cell

4. SRAM Block Structure

The basic SRAM block structure is as shown in figure 3. A row decoder gated by appropriate timing block signal decodes X row address bits and selects one of the word lines WL 0-WL N-1. The SRAM core consists of a number of arrays of NxM, where N is the number of rows and M is the number of bits. If an SRAM core is organized as a number of arrays in a page manner, an additional Z-decoder is needed to select the accessed page [1]. Figure 1 shows an example of SRAM with four pages of NxM arrays with the corresponding I/O blocks. SAM's can be organized as bit- oriented or word oriented. In a bit oriented SRAM, each address accesses a single bit, whereas in a word oriented memory, each address addresses a word of n bits (where the popular values of n include 8, 16, 32, or 64). Column decoders or column MUXs (YMUXs) addressed by Y address bits allow sharing of a single sense amplifier among 2, 4 or more columns. The majority of modern SRAMs are self timed, i.e. all the internal timing is generated by the timing block within an SRAM instance. An additional chip select signal, introducing an extra decoding hierarchy level, is often provided in multi-SRAM chip architectures.

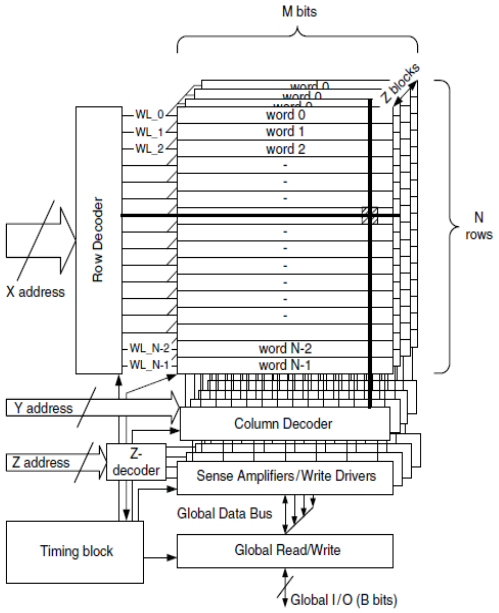

Fig. 3 SRAM block diagram

5. Conclusion:

An SRAM cell proposed offers reduced gate and sub threshold leakage currents and power in caches. In this paper an attempt is made to describe a CMOS VLSI design technology using SRAM as an example. The SRAM system can be developed using cadence, mentor graphics, microwind, ltspice software's etc.The SRAM design design schematic layout can be drawn and verified.

6. Scope For Future Work:

For further optimization and better performance this work can be carried out under lower CMOS technology such as 90nm, 45nm etc using different tools. And also much larger SRAM memory systems can be implemented.

7. References:

1. CMOS VLSI Design- a Circuits and systems perspective. Third edition-Neil H.E.WESTE, Macquarie university and the university of Adelaide , David HARRIS, Harvey Mudd College , Ayan Banerjee, Bengal Engineering and Science University.
2. Andrei Pavlov, Manoj Sachdev CMOS SRAM Circuit Design and Parametric Test in Nano-Scaled Technologies. Process-Aware SRAM Design and Test.
3. Leakage power estimation in SRAM'S by Mahesh Mamidipaka, Kamal Khouri, Nikhil Dutt, Magdy Abadir. CECS Technical Report#03-32.Centre for Embedded Computer Systems, University of California, Irvine, CA 92697, USA
4. M.D.Powell, S.H.Yang, B.Falsafi etal… Gated-VDD: A circuit technique to reduce leakage in cache memories. In proceedings of International Symposium on Low Power Electronics and Design, July 2000.
5. Tutorial cadence design environment by Antonio J.Lopez Martin.
6. S.Borkar.Design challenges of technology scaling.IEEE Micro, 19(4):23-29, august 1999.
7. T.Enomoto.Y.Oka and H.Shikano. self controllable voltage level (SVL) circuits, 38(7):1220-1226, july 2003.
8. Navid Azizi, Farid N.Najm.Andreas Moshovos.Low leakage asymmetric cell SRAM.IEEE transactions on VLSI systems, 11(4):701-715, August2003.